CHENGYI ZHANG

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EDUCATION

University of California, Berkeley, PhD, Electrical Engineering and Computer Science — In Progress

University of California, Berkeley, BA, Computer Science — Dec 2023
GPA: **3.980**/4 (Dean's List)

EXPERIENCE

CPU Platform Architecture Intern — May 2025 - August 2025
Apple — *Cupertino, CA*

- Worked on the identification of critical paths in the performance model.
- Worked on the analysis of the identified critical path to improve pipeline latency.

Student Researcher — July 2024 - August 2024
Google — *Sunnyvale, CA*

- Worked on memory access pattern synthesis via processor trace replay.

CPU Design Verification Intern — May 2023 - August 2023
Apple — *Cupertino, CA*

- Worked on verification coverage infrastructure for CPU design verification.
- Worked on verification suites for memory-subsystem securities for future products.

RESEARCH PROJECTS

TACIT, Timing Annotated Core Instruction Trace — Latest

- An open-source hardware trace encoder that encodes time elapsed between every basic block, to facilitate fine-grained time profiling post-silicon
- Towards using the profiling information to improve the profile-guided optimization flow in compilers

RoSÉ, HW-SW Cosimulation of Full-Stack Robotics SoC Evaluation Infrastructure

- Paper presented at *ISCA 2023*, and received Distinguished Artifact Award.
- Integrated the experimental FireSim on-premises FPGA deployment.
- Designed experiments sweeping across different software and hardware architecture for the optimal design points.

CoSMo, A Computing and Sensing I/O Device Model for Pre-Silicon Full-Stack SoC Evaluation

- Abstract, poster, and presentation presented at *MICRO 2023 Student Research Competition*, won third place.
- Designed and implemented parameterized sensor channel generator with various interface options.
- Designed and implemented near-sensor Dataflow systolic array Accelerators for stereo matching depth estimation, sobel edge detection, and Pool2D.

FireAxe, partitioning monolithic RTL designs in FireSim

- Paper presented at ISCA 2024, and received Distinguished Artifact Award.
- Established high-speed communication between Alveo U250 Accelerator Card FPGAs through Aurora protocol Vivado IP cores over QSFP ports and optical links.
- Extended the FireSim infrastructure to support communication over QSFP and successfully booted Linux.

- Evaluated the link round trip latency and simulation performance with a peak frequency of 1.6MHz.
- Extended the software simulation infrastructure to support direct-connect multi-FPGA debugging.

COURSE PROJECTS

UCIe Sideband, high speed chiplets interconnect standard in Chipyard *EECS251B: Advanced Digital Design*

- Designed and Implemented the sideband channel and relevant modules.
- Designed and Implemented utilities for parsing sideband messages and factory methods for Chipyard Integration
- The Project received the 2023 Apple Class Design Award.

TPGO, trace-driven profile guided optimization *CS265: Compiler Optimization*

- Implemented a flow of converting trace data into basic-block level information to perform PGO
- Evaluated and compared with the sota GCC PGO flow and AutoFDO, report available here

Fireflower, Learning-based basic-block level performance prediction *EE244: Systems Modeling*

- Trained a transformer for inferencing on latency attribution of timestamp augmented trace
- Evaluated the strength and identified the weakness of this approach, report available here

LCD Driver, high performance, low-power analog driver for LCD Display *EE140: Analog Design*

- Designed an analog folded telescopic differential amplifier for driving an RC-modeled LCD Display matrix.
- Reached a low power consumption of 0.542mW and a settling error of 0.105% within 180ns delay.

RV32I CPU, single-core in-order RISC-V processor *EECS151: Digital Design*

- Designed and implemented a CPU with RISC-V instruction set architecture and a 3-stage pipeline in Verilog, pushed through physical design flow with ASAP-7nm technology.
- Implemented a direct-mapped, write-back cache.

PUBLICATION

RoSÉ: A Hardware-Software Co-Simulation Infrastructure Enabling Pre-Silicon Full-Stack Robotics SoC Evaluation
Dima Nikiforov, Shengjun Chris Dong, **Chengyi Lux Zhang**, Seah Kim, Borivoje Nikolic, Yakun Sophia Shao
International Symposium on Computer Architecture (ISCA), June 2023
ISCA Distinguished Artifact Award
Artifacts Available, Artifacts Evaluated - Functional, Results Reproduced

FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs
J. Whangbo, E. Lim, **C. Zhang**, K. Anderson, A. Gonzalez, R. Gupta, N. Krishnakumar, S. Karandikar, B. Nikolic, S. Shao, K. Asanovic
International Symposium on Computer Architecture (ISCA), June 2023
Artifacts Available, Artifacts Evaluated - Functional, Results Reproduced

TEACHING EXPERIENCE

Academic Student Employee Jan 2022 - Present
UC Berkeley *Berkeley, CA*

- Course **Teaching Assistant,** EECS151: Digital Design, Spring 2023: student rating *6.97/7*; Fall 2023.
- Course **Reader**, EECS151: Digital Design, Fall 2022.
- Computer Science Mentor, Junior Mentor, CS61C: Intro to Machine Structures, Spring 2022.